FORM PTO-1390 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NO. FR 000072
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. Application No. (if known, see 37 CFR 1.5) 10/069536
INTERNATIONAL APPLICATION NO. PCT/~~EP99/07014~~ EP01/07406	INTERNATIONAL FILING DATE September 17, 1999	PRIORITY DATE CLAIMED October 5, 1998
TITLE OF INVENTION SELF-CONFIGURABLE AMPLIFIER CIRCUIT		
APPLICANT(S) FOR DO/EO/US GILLES CHEVALLIER		

Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.

2. [ ] This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.

3. [X] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. [ ] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. [X] A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. [X] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).

6. [ ] A translation of the International Application into English (35 U.S.C. 371(c)(2))

7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.

8. [ ] A translation of the amendment to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).

9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. To 16. Below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98.

12. [X] An assignment document for recording. A separate cover sheet is compliance with 37 C.F.R. 3.28 and 3.31 is included.

13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND OR SUBSEQUENT preliminary amendment.

14. [ ] A substitute specification.

15. [X] A change of power of attorney and/or address letter.

16. [X] Other items or information:
    6 Sheets of formal drawing
    Authorization under 37 CFR 1.136 (a) (3)

CERTIFICATE OF MAILING

Express Mail Mailing Label No. EL 686950412 US
Date of Deposit: February 25, 2002
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks Washington, D.C. 20231.

Edna Chapa
Typed Name

Signature

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U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 10/069536	INTERNATIONAL APPLICATION NO. PCT/EP01/02906	ATTORNEY'S DOCKET NUMBER FR 000026

17 [X] The following fees are submitted:		CALCULATIONS (PTO USE ONLY)
BASIC NATIONAL FEE (37 C.F.R. 1.492(A)(1)-(5)):		
Search Report has been prepared by the EPO or JPO	$ 690.00	
International preliminary-examination fee paid to USPTO (37 C.F.R. 1.482)	$ 710.00	
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2)	$1040.00	
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2)) paid to USPTO	$ 100.00	
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	$ 860.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 690.00	$

Surcharge of $130.00 for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	10 - 20 =		X $ 18.00	$	
Independent claims	2 - 3 =		X $ 84.00	$	
MULTIPLE DEPENDENT CLAIMS (if applicable)			+ $280.00	$	
TOTAL OF ABOVE CALCULATIONS			=	$ 690.00	
Reductions by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 C.F.R. 1.9, 1.27, 1.28)				$	
SUBTOTAL			=	$ 690.00	
Processing fee of $130.00 for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 C.F.R. 1.492(f)).			+	$	
TOTAL NATIONAL FEE			=	$ 690.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28,3.31). $40.00 per property			+	$ 40.00	
TOTAL FEES ENCLOSED			=	$ 730.00	
				Amount to be Refunded	$
				Charged	$

a. [ ] A check in the amount $_____ to cover the above fees is enclosed.

b. [X] Please charge my Deposit Account No. 14-1270 in the amount of $730.00 to cover the above fees.

c. [X] The Commissioner is hereby authorized to charge any additional fee, with the exception of the Base Issue Fee, which may be required, or credit any overpayment to Deposit Account No. 14-1270.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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32,266
(REGISTRATION NUMBER)

DATE OF MAILING: February 25, 2002

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Self-configurable amplifier circuit

Field of the invention

The invention relates to the field of tuners. The invention also relates to devices wherein such tuners are implemented, such as television receivers, video recorders or decoder boxes. The invention more particularly relates to an amplifier circuit comprising:

- a pre-amplifying stage,
- an amplifying stage, and
- identification means for identifying the configuration of the amplifying stage.

Prior art

Such an amplifier circuit is known from the PCT patent application published under publication no. WO 00/21193.

According to this patent application, when an amplifying stage 511 is configured so as to be in the asymmetrical mode, i.e. when different outputs of this amplifying stage are connected together, a commutator Sw controlled by control means 53 connects one of the outputs O_2 of the amplifying stage 511 to ground. A configuration in an asymmetrical mode of an amplifying stage optimized for operation in the symmetrical mode causes a deterioration of the amplification characteristics. The magnitude of this deterioration can be limited to some extent by connecting one of the outputs of the amplifying stage to ground.

In an improved variant, as shown in Fig. 2 of said patent application, commutation means 2513 comprise two commutators. When the amplifying stage 2511 is configured so as to be in the symmetrical mode, a first commutator SW 22 is open so that the gain of the amplifier circuit is determined by a first set of resistors R_1, R_2 and R_4. When the amplifying stage 2511 is configured so as to be in the asymmetrical mode, a single output branch of the amplifying stage is used, and it is suitable to increase the gain of said branch. For this purpose, the commutator SW 22 is in the closed state and a resistor R_3 is introduced into the circuit, thereby increasing the gain of the branch that is still being used.

Said patent application does not indicate how the controller 53 is controlled so as to either activate or not activate the commutation means SW, SW_{21}, SW_{22}. Persons skilled in the art are also well aware of the fact that the modification of the amplifier circuit intended to limit

the deterioration of the amplification characteristics only palliates this deterioration, and that the correction is not the optimum that can be achieved in the asymmetrical mode.

Brief description of the invention

It is an object of the invention to overcome the drawbacks described hereinabove by providing an amplifier circuit which can suitably be configured, in a flexible manner, so as to be in the symmetrical or asymmetrical mode, the performance of the circuit being automatically optimized irrespective of the mode of operation of the circuit resulting from its configuration.

Thus, in accordance with the invention, an amplifier circuit in accordance with the opening paragraph is characterized in that it additionally comprises adaptation means to configure the pre-amplifying stage in such a manner that it supplies the amplifying stage with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

By virtue of the invention, in either mode of operation, i.e. the symmetrical or asymmetrical mode, the performance of the amplifier circuit as regards gain, linearity and output impedance meets the expectations of a circuit optimized for operation in said mode. Thus, unlike the prior art, it is not merely a limitation of the degradation in performance resulting from a configuration other than the configuration for which the amplifier circuit has been designed, but instead an optimization of each one of the configurations.

In the amplifier circuit in accordance with the prior art, a part of the amplifying stage is deactivated during operation in the asymmetrical mode, the gain of the other part being then increased. In accordance with the invention, the whole amplifying stage is used to full advantage to generate the output signal of the amplifier circuit, irrespective of the configuration chosen.

Thus, in its most general mode, the invention relates to a method of optimizing the operation of an amplifier circuit, comprising:

- a pre-amplifying stage, and
- an amplifying stage,

which method includes an identification step for identifying the configuration of the amplifying stage, characterized in that the method additionally comprises a configuration step

for configuring the pre-amplifying stage, as a result of which the amplifying stage is supplied with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

In accordance with an embodiment of the invention, the pre-amplifying stage may comprise two pre-amplifiers, which are both arranged between two inputs of the amplifier circuit and two inputs of the amplifying stage, the adaptation means alternately activating one of the two pre-amplifiers and deactivating the other.

The first pre-amplifier amplifies the input signal in such a way that the signals present at each one of the outputs are in phase opposition with respect to one another. The second pre-amplifier amplifies the input signal in such a way that the signals present at each one of the outputs of the pre-amplifying stage are in phase.

Brief description of the drawings

Other advantages will be apparent from the description of an embodiment of the invention, which description is given with reference to the annexed drawings, wherein:

- Fig. 1 is a functional diagram of a receiver of radioelectric signals, wherein the invention is implemented;
- Fig. 2 is a functional diagram of a tuner included in such a receiver;
- Fig. 3 is a functional diagram of an embodiment in accordance with the invention;
- Fig. 4 is an electrical circuit diagram of an embodiment of a part of the identification means for identifying the configuration of the amplifying stage;
- Fig. 5 is an electrical circuit diagram of an embodiment of another part of identification means for identifying the configuration of the amplifying stage;
- Fig. 6 is a synthesis diagram of Figs. 3 to 5;

In each one of the drawings, like reference numerals refer to like parts.

Description of an embodiment in accordance with the invention

Fig. 1 diagrammatically shows a receiver for receiving radioelectric signals, for example a television receiver, which comprises, downstream of an input stage, constituent in this example by an antenna 1:

- an amplifier 2 receiving the antenna signal through one or several passband filters 3, and

- a tuner 5 receiving, through the filters 4, a signal originating from the amplifier 2.

The tuner 5 supplies an output signal having an intermediate frequency.

Usually, a tuner doesn't comprise only a single chain composed of the elements 2 through 4. A tuner often comprises additional chains, diagrammatically represented in this example by reference numerals 6 and 7.

Each one of the chains can be tuned to a particular frequency included in a band of operation of the chain.

The intermediate frequency IF at the output of the tuner 5 is always the same. Its value generally lies between 30 and 60 MHz.

Fig. 2 diagrammatically shows a tuner 5 comprising a mixer 8 receiving, at an input 9, the amplified antenna signal and, at an input 10, a signal originating from a local oscillator 11. The frequency of the oscillator 11 is controlled by a phase-locked loop 12, which itself is controlled, through a bus 13, by a microcontroller 14.

The output 15 of the mixer 8 conveys an intermediate frequency signal, which can be transmitted in one or several channels, for example, in the single sideband (SSB). If there are several channels, the signal is introduced, for example, at a surface wave filter 16 which is intended to separate the channels. In accordance with a first variant, which is generally used in Europe, the surface wave filter 16 is a high-impedance filter, for example 500 Ω, and the introduction of the signal takes place through a passband filter 17. In accordance with a second variant, which is more generally used in Asia and indicated by means of dashed lines, the output signal 15 of the mixer 8 is amplified by an amplifier 18 before being introduced into the acoustic wave filter 16 having an output 20.

One or several wall filters, such as the one bearing reference numeral 19, which is used for trapping certain frequencies, may be used for filtering the output signal 15.

In the application described hereinabove, the circuit in accordance with the invention is arranged downstream of the tuner 5.

Fig. 3 shows an amplifier circuit 50 in accordance with a particular embodiment of the invention, said amplifier circuit having two inputs 20, 20' and two outputs 28, 28'. The circuit 50 comprises a pre-amplifying stage 41, two inputs of which are connected to inputs 20, 20' of the amplifier circuit, and two outputs 27, 27' of which are connected to two inputs of the amplifying stage 42 comprising two amplifiers 22, 22'.

The pre-amplifying stage 41 comprises a first and a second pre-amplifier 31, 44 which are arranged in parallel between the inputs 20, 20' and the outputs 27, 27' of the pre-amplifying stage. The outputs of the first pre-amplifier 31 convey signals which are in phase opposition.

The outputs of the second pre-amplifier 44 carry signals which are in phase. The two pre-amplifiers 31, 44 never operate simultaneously; they operate alternately according to the configuration of the amplifying stage 42. The second pre-amplifier 44 is itself composed of two parts 21, 21'.

Each part 31, 21 and 21' comprises a long-tail pair of transistors (23, 24); (23', 24'); and (23", 24"), respectively, the control terminals of which are formed by the bases of said transistors, and an output terminal of which is formed by the collector of one of the transistors of the long-tail pair. The bases of the transistors 23, 23' and 23" are connected to the input 20, while the bases of the transistors 24, 24' and 24" are connected to the inputs 20'. As the control terminals of the long-tail pairs (23', 24') and (23", 24") included in the second pre-amplifier 44 are identically coupled for both long-tail pairs, the outputs 27 and 27' of the second pre-amplifier 44 supply current signals which are in phase. In addition, the gains of the long-tail pairs (23, 24), (23', 24'), (23", 24") included in the pre-amplifiers 31 and 44 can be advantageously made variable so as to enable an increase of the flexibility of the amplifier circuit. This can be achieved by choosing variable current sources to bias said long-tail pairs, according to a technique which is well known to those skilled in the art.

Though, in this example, bipolar-type transistors are employed, these transistors can be substituted with MOS-type transistors, the grids of which would then form the control terminals. The two amplifiers 22 and 22' are used simultaneously irrespective of which one of the pre-amplifiers 31 or 44 is activated.

The configuration of the pre-amplifying stage 41 is carried out as follows:

In the embodiment discussed herein, the first symmetrical output pre-amplifier 31 is selected by default. Of course, it is also possible to select the second pre-amplifier 44 by default.

The connection of outputs 28, 28' of the amplifier circuit 50 in the short-circuit configuration, i.e. in the asymmetrical mode, or to a load impedance, i.e. in the symmetrical mode, is most often definitively performed by the manufacturer of the apparatus which incorporates said amplifier circuit. The amplification circuit 50 is provided with identification means 45 of the configuration as the amplifying stage 42, which identification means are parallel connected to a load impedance, not shown in the drawing, between the outputs 28 and 28'.

The identification means 45 produce a so-called selection signal, the value of which enables the presence of a weak load impedance to be identified, i.e. a load impedance value below a predetermined threshold, or the presence of a standard load impedance corresponding to a situation wherein the amplifier circuit 50 is configured so as to be in the symmetrical mode. The selection signal is transmitted to adaptation means 46.

If the selection signal indicates that the amplifying stage 42 is not configured to operate in the symmetrical mode, i.e. using the pre-amplifier 31 provided by default, then the adaptation means 46 are activated by the selection signal. If the adaptation means are activated, they cause the transistors (23, 24) of the first pre-amplifier 31 to become deactivated, and the transistors (23', 24'); (23", 24") of the second pre-amplifier 44 to become activated. Activation or deactivation of the transistors is obtained by, respectively, activating or deactivating the current sources biasing these transistors.

Figs. 4 and 5 show an embodiment of identification means 45.

Fig. 4 shows detection means 60 included in the identification means 45. In Fig. 4, the amplifiers 22 and 22' are shown, said amplifiers each having an output resistor Rs 47, 47' arranged between a point 51, 51' and the output 28, 28', respectively. A load impedance RL is assumed to be arranged between the two outputs 28 and 28'. The detection means shown in Fig. 4 comprise a first and a second main branch 48 and 48', respectively. The first main branch 48 comprises three branches 52, 53 and 54. An end of a branch 52 is connected to an output 55 of the branch 48. Said branch comprises a transistor, the collector of which is connected to the output 55, and the emitter of which is connected, through a resistor Rm, to the connection 51 opposite the output 28 of an output resistor 47 of the amplifier 22. A central branch 53 comprises a transistor arranged in a diode configuration, a collector connected to the base, arranged in series with a resistor Rc arranged between the collector of the transistor and a bias-voltage source, and in series with a resistor Rm arranged between the emitter of the transistor and the output 28. A branch 54 is identical to the branch 52. The collector of the transistor of the branch 54 is connected to the output 55 of the branch 48, and the emitter is connected, through a resistor of value Rm, to the output 28' of the amplifier 22'.

The second main branch 48' of these detection means 60 included in the identification means 45 and the branch 48 are symmetrical with respect to an imaginary center point 0 of the load resistor RL, thereby dividing the load resistor RL in two half resistors having a value RL/2 each. The resistor RL is intended to produce an output voltage, referenced Vout, having a DC component, referenced $Vout_{dc}$, and an AC component, referenced $Vout_{ac}$.

In an idle state, i.e. in the absence of the AC component $Vout_{ac}$, the branch 54 is a current mirror of the branch 53.

If an AC component $Vout_{ac}$ appears at the terminals of the load resistor RL, the resistor Rm of the branch 54 is subjected to an additional voltage resulting in an additional current

$i' = Vout_{ac}/Rm$. With respect to the rest of the explanation, it is to be noted that if Rc is much larger than Rm, the idle current i, which is equal to $Vout_{dc}/(Rc+Rm)$, is much smaller than i'. For example, if Rc = 10 Rm, then i' is more than ten times larger than i. As a result, it is possible to disregard the idle current i in the rest of the explanations. If it is assumed that RL/2 is equal to the sum of the output resistances Rs, then a current i" present in the branch 52 is equal to i'. In this case, the current at the output 55 of the branch 48 is zero.

If it is assumed that RL is much larger than Rs, then the current i' in the branch 54 is much larger than the current i" in the branch 52. In this case, the direction of the current at the output 55 is the same as that of the current i' in the branch 54. The same result is obtained for the branch 48'. The current at the output 55' flows in the same direction as the current i' in the branch 54'. If RL is much smaller than Rs, which corresponds particularly to a short-circuit between the outputs 28 and 28', the current i' in the branch 54 is smaller than the current i" in the branch 52. In this case, at the output, there is a current that flows in the same direction as the current i" in the branch 52. This is also true for the branch 48'.

Thus, depending on the relative value of the resistors RL and Rs, the direction of flow of the current present at the output 55, 55' of the branches 48 and 48' is either the same as or opposite to the direction of flow of the current at the output of the amplifiers 22, 22'.

A comparison between the direction of flow of the current at the output 55, 55' and the direction of flow of the current at the output of the amplifiers 22, 22' indicates whether the amplifier circuit is connected in the symmetrical mode or the asymmetrical mode. For a better understanding of the circuit, some numerical values will be given hereinbelow by way of example. The resistances Rm and Rc may be of the order of 4 kΩ and 40 kΩ, respectively. If a load impedance of 500 Ω is connected to two outputs 28, 28' which are mutually short-circuited by a short-circuit of 2 Ω, corresponding to a welding capacity of 1 nanofarad, a current of 25 μA is obtained, for an amplitude of the output voltage of 100 mV, at the output 55, 55', which is amply sufficient to activate logic circuits included in the adaptation means. These values show that the output signal Vout is not in the least disturbed by the detection means 60.

Fig. 5 shows selection means 70 included in the identification means 45. These selection means are intended to generate a current, forming the selection signal, the direction of which is always the same and depends only on the relative values of the resistances RL and Rs. This circuit comprises two outputs K, K'. Depending on the relative values of the resistances RL and Rs, only one of these two outputs is energized.

The selection means 70 comprise a GILBERT cell 59 including a first and a second pair 61, 61' of NPN transistors 57, 58 and 57', 58' respectively.

The selection means additionally comprise a PNP transistor 63 arranged in a diode configuration, the base and the collector of which are connected to an output 55 of the above-described detection means. Two PNP transistor 64, 65 are arranged in a current-mirror configuration with the transistor 63. The collector of the transistor 64 is connected to a collector of an NPN transistor 66 which is arranged in a diode configuration. The collector of the PNP transistor 65 is connected to the common emitter of the second pair 61' of the transistors 57', 58' of the GILBERT cell 59. The selection means 70 comprise, in a symmetrical manner, a PNP transistor 63' arranged in a diode configuration, the base and the collector of which are connected to another output 55' of the detection means described with respect to Fig. 4. Two transistors 65' and 64' are arranged in a current-mirror configuration with the transistor 63'. The collector of the PNP transistor 64' is connected to the collector of an NPN transistor 66' arranged in a diode configuration. The collector of the transistor 65' is connected to the common emitters of the transistors 57, 58 of the first pair 61 of the GILBERT cell 59.

The collectors of a first transistor 57, 57' of each pair 61, 61' are connected to a point K forming an output of the circuit 70, and the collectors of a second transistor 58, 58' of each pair 61, 61' are connected to a point K' forming another output of the circuit 70.

The common emitters of the transistors of each pair 61, 61' are connected to, respectively, the NPN transistors 67, 67', said transistors 67, 67' being arranged in a current-mirror configuration with the transistors 66 and 66', respectively.

The base of the first transistor 57 of the pair 61 and the base of the second transistor 58' of the pair 61' are jointly connected to the output 28 of the amplifying stage.

The base of the second transistor 57' of the pair 61' and the base of the first transistor 58 of the first pair 61 are jointly connected to the output 28' of the amplifying stage.

Resistors, not shown in the drawing, may be inserted between the output terminals 28, 28' and the bases of the transistors (57, 58') and (57', 58), respectively, to improve the linearity of the GILBERT cell 59.

The operation of the selection means 70 is as follows:

If it is assumed that a current signal is supplied by the outputs 55, 55' of the detection means 60, then only one of the outputs K or K' supplies a current. If, at the time of a subsequent alternation, the current signal supplied by the outputs 55, 55' of the detection means 60 changes direction, the biasings of the bases of the transistors 57, 58' and 57', 58 of the

GILBERT cell received from the outputs 28, 28' are also inversed, so that the current at the output of the cell 59 is present at the same output K or K' than at the time of the preceding alternation.

Thus, depending on whether the load resistance RL present between the outputs 28 and 28' is larger than the output resistance Rs of the amplifiers 22, 22', or, conversely, smaller than said output resistance Rs of the amplifiers 22, 22', one of the outputs K or K' supplies a current, for example output K if RL << Rs, or output K' in the opposite case.

Fig. 6 diagrammatically shows again the assembly shown in Fig. 3 to illustrate the connections between the different parts of the amplifier circuit 50.

The outputs 51, 28, 51', 28' of the stage 42 form inputs for the detection means 60 included in the identification means 45. The selection means 70, which form part of the identification means 45, receive the current originating from the outputs 55, 55' of the detection means 60. The outputs K, K' of the selection means 70 generate the selection signal, which is applied to a memory flip-flop included in the adaptation means 46. Outputs Q and Qnot of this memory flip-flop supply activation or deactivation signals intended to be applied in return to the pre-amplifying stage 41 of the amplifier circuit 50.

If, in the example described hereinabove, the selection signal is such that the output K is activated and the output K' is deactivated, this means that the value of the load resistance RL is very small as compared to that of the resistances Rs, i.e. the amplifying stage 42 is configured so as to be in the asymmetrical mode. The outputs Q and Qnot of the adaptation means 46 then enter the active or inactive state, represented, for example, by the logic levels 1 and 0, respectively, thereby activating the current sources biasing the long-tail pairs of the second pre-amplifier 44 and deactivating the long-tail pair of the first pre-amplifier 31.

CLAIMS:

1. An amplifier circuit comprising:

- a pre-amplifying stage,
- an amplifying stage, and
- identification means for identifying the configuration of the amplifying stage,

which circuit is characterized in that it additionally comprises adaptation means to configure the pre-amplifying stage in such a manner that it supplies the amplifying stage with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

2. An amplifier circuit as claimed in claim 1, characterized in that the pre-amplifying stage comprises two pre-amplifiers, which are both arranged between two inputs of the amplifier circuit and two inputs of the amplifying stage, the adaptation means alternately activating one of the two pre-amplifiers and deactivating the other.

3. An amplifier circuit as claimed in claim 2, characterized in that the pre-amplifying stage includes a first pre-amplifier comprising two transistors forming a long-tail pair, having control terminals which are connected to inputs of the amplifier circuit.

4. An amplifier circuit as claimed in claim 2, characterized in that the pre-amplifying stage includes a second pre-amplifier comprising four transistors which, arranged two-by-two, form a first and a second long-tail pair, having control terminals which are connected in parallel to inputs of the amplifier circuit, each long-tail pair having an output connected to one of the inputs of the amplifying stage.

5. An amplifier circuit as claimed in claim 1, characterized in that the identification means of the amplifying stage configuration comprise detection means connected to the outputs of said amplifying stage, said detection means having at least one

output intended to supply a current whose direction is determined univocally by the direction of an output current generated by the amplifier circuit.

6. An amplifier circuit as claimed in claim 5, characterized in that the identification means of the amplifying stage configuration comprise selection means connected to the detection means and having two outputs intended to be energized alternately according to the direction of the current supplied by the outputs of the detection means.

7. An amplifier circuit as claimed in claim 1, characterized in that the adaptation means comprise a flip-flop intended to store information provided by the identification means, a logic output of said flip-flop being coupled to the pre-amplifying stage.

8. A tuner characterized in that it includes an amplifier circuit as claimed in claim 1.

9. A receiver for receiving radioelectric signals, characterized in that it includes a tuner as claimed in claim 8.

10. A method of optimizing the operation of an amplifier circuit comprising

- a pre-amplifying stage, and
- an amplifying stage,

which method comprises an identification step for identifying the amplifying stage configuration, characterized in that the method additionally includes a configuration step to configure the pre-amplifying stage in such a manner that it supplies the amplifying stage with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

ABSTRACT:

The invention relates to an amplifier circuit 50 comprising:

- a pre-amplifying stage 41,
- an amplifying stage 42, and
- identification means 45 for identifying the configuration of the amplifying stage 42.

In accordance with the invention, adaptation means 46 enable to configure the pre-amplifying stage 41 in such a manner that it supplies the amplifying stage 42 with:

- either two signals which are in phase opposition if the amplifying stage is configured so as to be in the symmetrical mode,
- or two signals which are in phase if the amplifying stage is configured so as to be in the asymmetrical mode.

The invention enables an amplifier to be configured in the symmetrical or asymmetrical mode, in a flexible manner, the performance of said amplifier being optimal irrespective of the configuration chosen.

Application: Amplification of tuner output signals.

Reference: Fig. 3

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

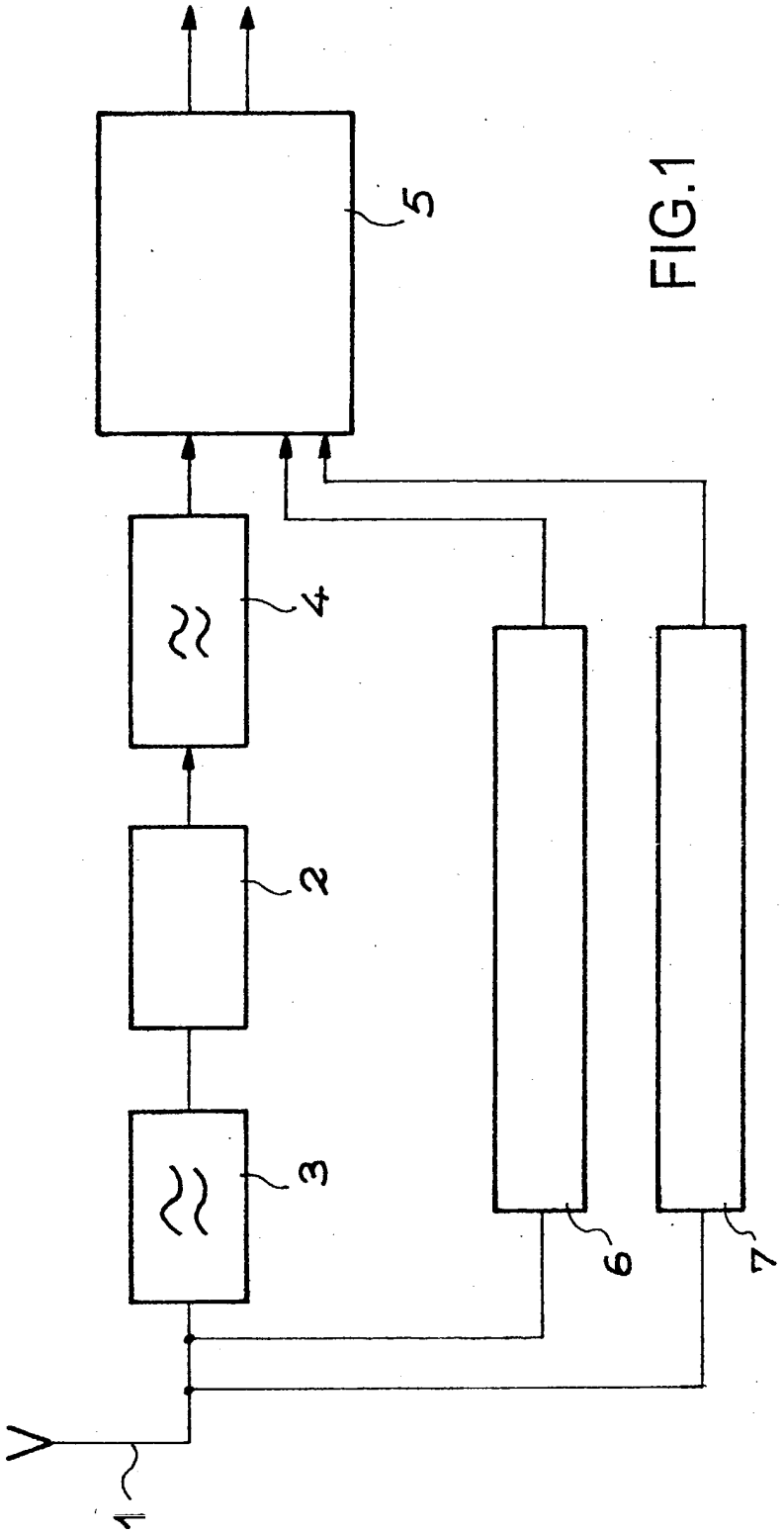

FIG.1

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

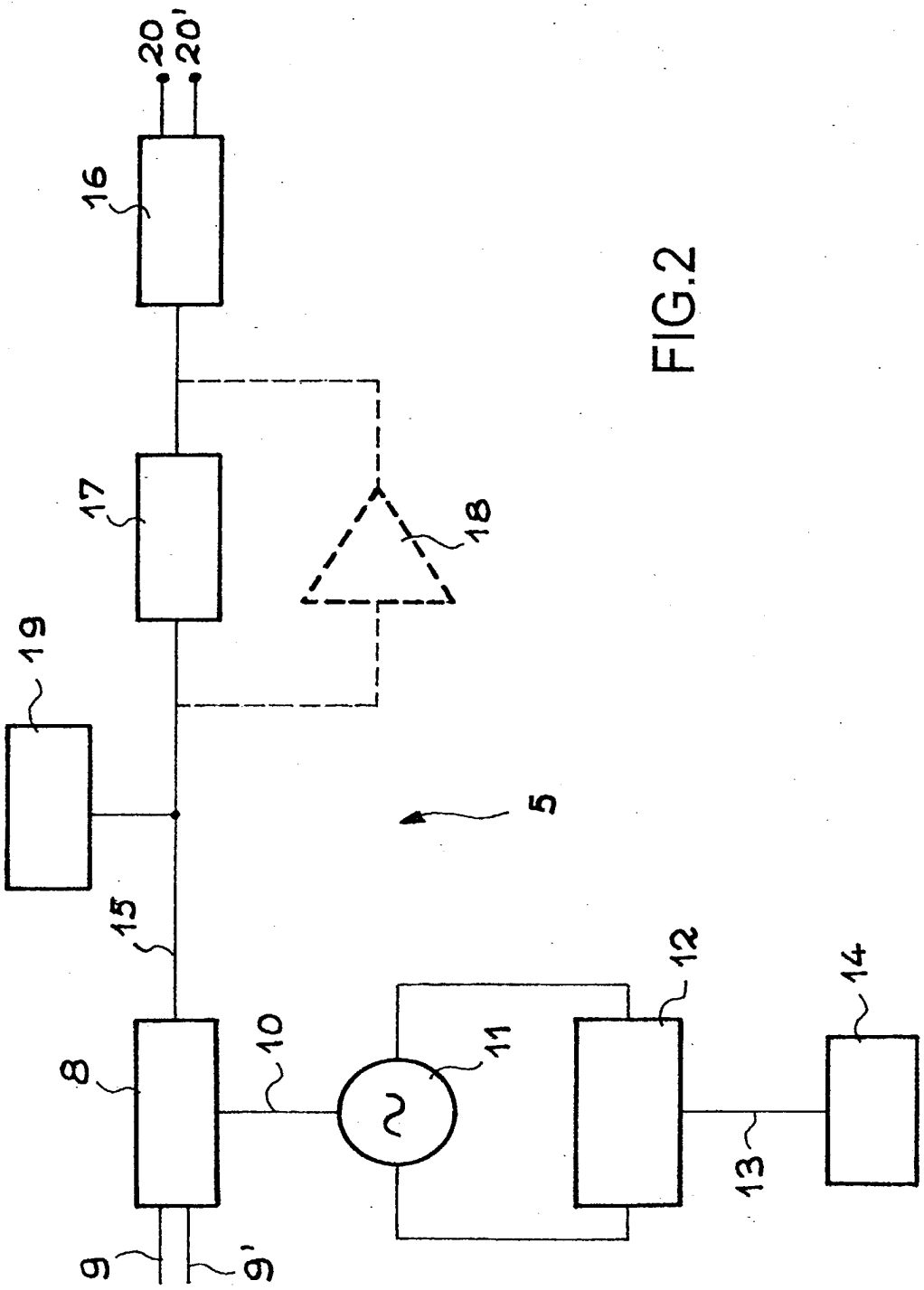

FIG.2

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

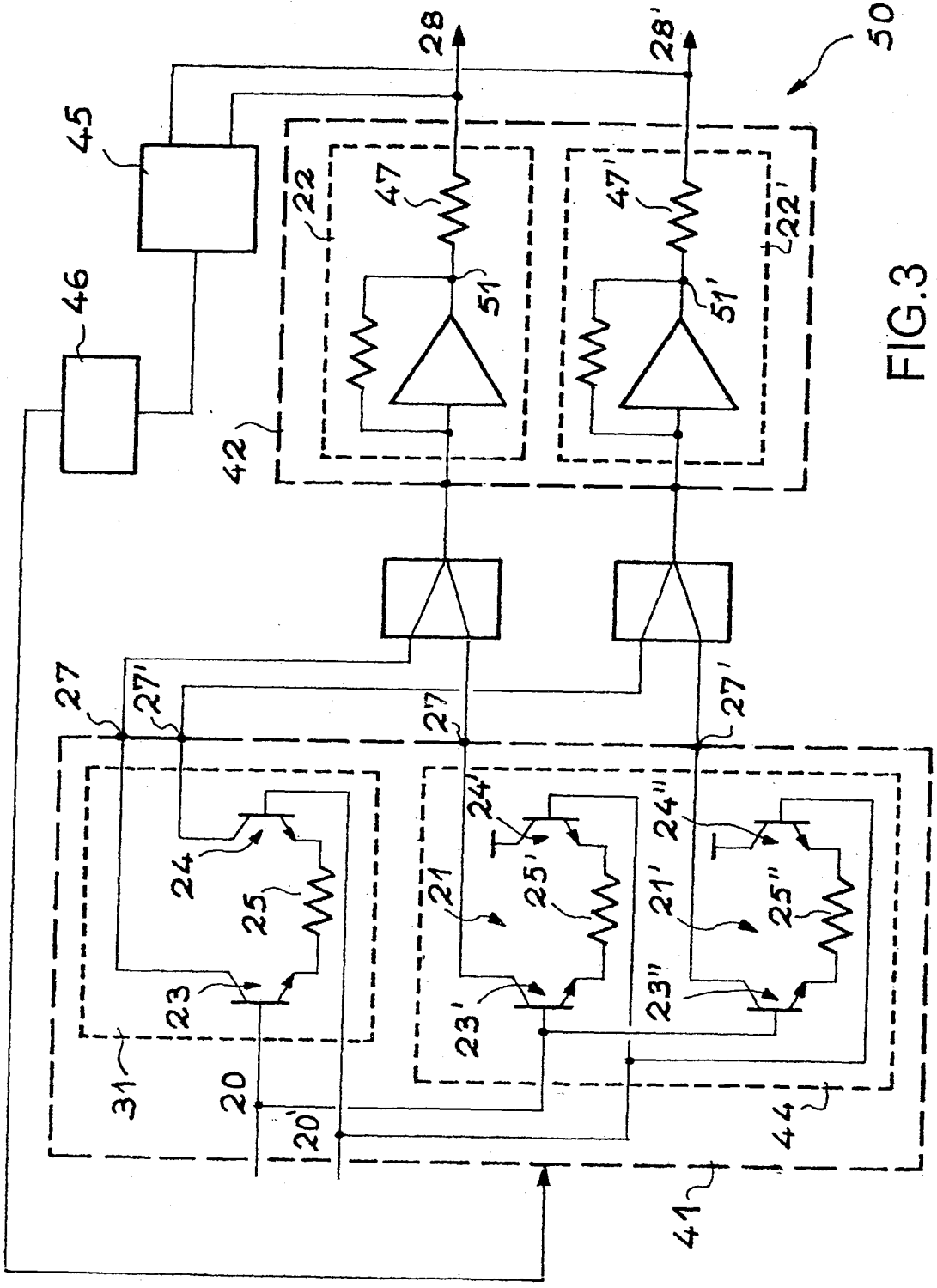

FIG.3

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

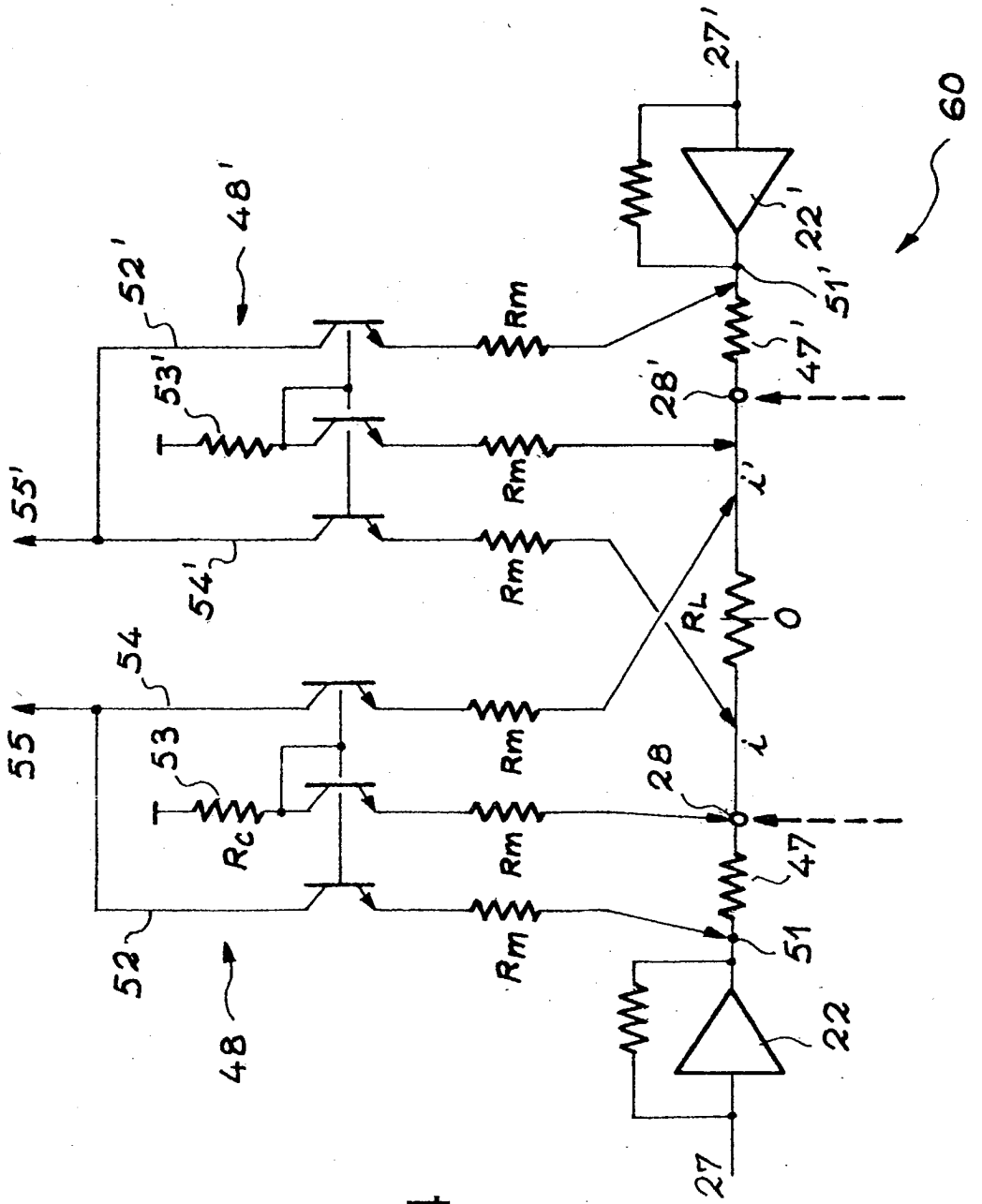

FIG.4

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

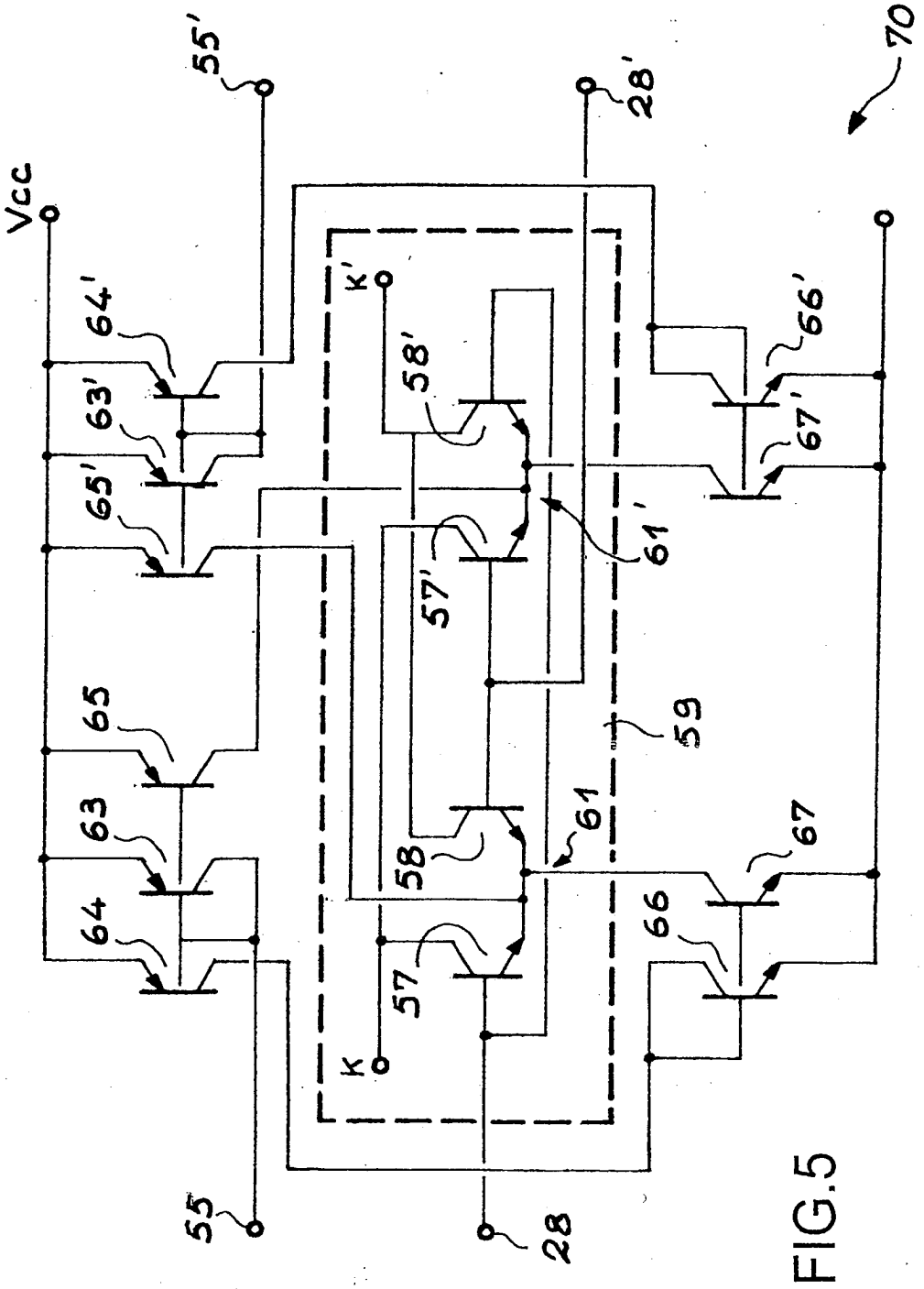

FIG.5

INVENTOR: GILLES CHEVALLIER
Attorney Docket: PHFR 000072
Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT
Contact: STEVEN R. BIREN 914) 333-9630

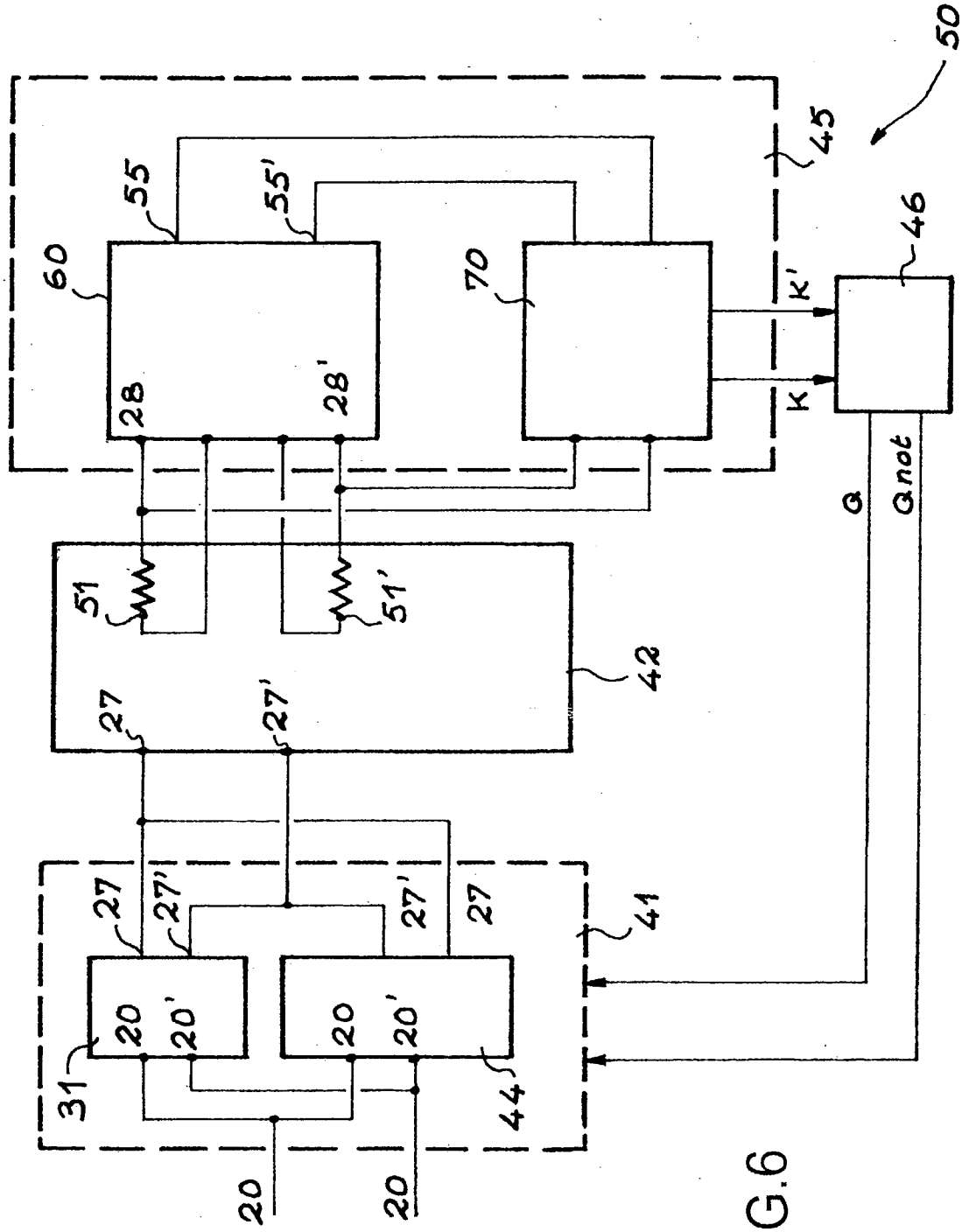

FIG.6

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER **PHFR000072 US**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **"Self-configurable amplifier circuit"**
the specification of which (check only one item below):

☐ is attached hereto.

☐ was filed as United States application

Serial No _____

on _____

and was amended

on _____

☒ was filed as PCT international application

Number PCT/EP01/07406

on 28 June 2001

and was amended under PCT Article 19

on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 USC 119
France	**0008542**	**30 June 2000**	**YES**

ombined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT International Applications)	Attorneys Docket Number **PHFR000072 US**
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) abnd/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)	
Jack E. Haken, Reg. No. 26,902 Michael E. Marion, Reg. 32,266 Edward M. Blocker, Reg. No. 30,245	Direct Telephone Calls to: (name and telephone number) (914)332-0222

60	FULL NAME OF INVENTOR	FAMILY NAME **CHEVALLIER**	FIRST GIVEN NAME **Gilles**	SECOND GIVEN NAME
201	RESIDENCE & CITIZENSHIP	CITY **Langrune/Mer**	STATE OR FOREIGN COUNTRY **France**	COUNTRY OF CITIZENSHIP **France** FRX
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **Rue des Tulipes**	CITY **FR-14830 Langrune/Mer**	STATE & ZIP CODE/COUNTRY **France**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 if Title 18 of the United states Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201

S Chevallier

DATE 17 January 2002

U.S. DEPARTMENT OF COMMERCE- Patent and Trademarks Office
(July 1994)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of GILLES CHEVALLIER

Atty. Docket PHFR 000072

Serial No.:

Filed: CONCURRENTLY

Title: SELF-CONFIGURABLE AMPLIFIER CIRCUIT

Commissioner for Patents
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

STEVEN R. BIREN **(Registration No. 26,531)**

c/o PHILIPS ELECTRONICS NORTH AMERICA CORPORATION, Corporate Intellectual Property, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Michael E. Marion, Reg. 32,266
Attorney of Record

Dated at Tarrytown, New York
on February 25, 2002.

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